Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-9. (canceled)

10. (original) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material.

11. (currently amended) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material;

~~The method, according to claim 10,~~ wherein:

the spacer is made porous by exposing the spacers to an oxygen plasma.

12. (currently amended) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material;

~~The method, according to claim 10,~~ wherein:

the spacer comprises organic material; and

the spacer is made porous by removing the organic material.

13. (currently amended) The method, according to claim 10, wherein:

the spacer comprises a Si-O-C-N type of low-k material.

14. (currently amended) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material;

~~The method, according to claim 10,~~ wherein:

the pores are formed during the spacer etch, rather than during deposition of the dielectric material.

15. (original) The method, according to claim 10, wherein the spacer has a reduced dielectric constant (k).

16. (original) The method, according to claim 15, wherein the reduced dielectric constant (k) is less than 3.85.

17. (currently amended) A method of forming a spacer for a gate electrode of a transistor comprising the steps:

depositing a dielectric material;

etching the dielectric material to form a spacer;

forming pores in the dielectric material; and

depositing a thin layer over the porous dielectric material;

wherein the spacer has a reduced dielectric constant (k);

~~The method, according to claim 15,~~ wherein the reduced dielectric constant (k) is less than 7.0, but greater than 3.85.

18. (original) The method, according to claim 15, wherein the spacer is porous, and further comprising depositing a thin layer on the spacer to prevent moisture aborption.

19. (original) The method, according to claim 10, wherein the thin layer comprises oxide.

20. (original) The method, according to claim 10, wherein the thin layer has a thickness of less than 5nm.

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21. (new) The method, according to claim 11, wherein:
the spacer comprises a Si-O-C-N type of low-k material.

22. (new) The method, according to claim 14, wherein:
the spacer comprises a Si-O-C-N type of low-k material.

23. (new) The method, according to claim 17, wherein:
the spacer comprises a Si-O-C-N type of low-k material.

24. (new) The method, according to claim 11, wherein:
the spacer has a reduced dielectric constant (k); and
the reduced dielectric constant (k) is less than 3.85.

25. (new) The method, according to claim 14, wherein:
the spacer has a reduced dielectric constant (k); and

the reduced dielectric constant (k) is less than 3.85.

26. (new) The method, according to claim 17, wherein:

the spacer has a reduced dielectric constant (k); and

the reduced dielectric constant (k) is less than 3.85.

27. (new) The method, according to claim 11, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride.

28. (new) The method, according to claim 14, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride.

29. (new) The method, according to claim 17, wherein the thin layer comprises a material selected from the group consisting of oxide, amorphous silicon and nitride.

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